Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims

1. (Cancelled) A method for forming at least one nonvolatile memory device, comprising the following steps:

(a) forming a trapping layer on a prepared substrate;

(b) forming a patterned photoresist layer on the trapping layer;

(c) using the photoresist layer as an implanting mask to perform an implantation to form at least one bit line;

(d) forming a first material layer on surfaces of the photoresist layer;

(e) using the first material layer as an etching mask to pattern the trapping layer into at least one trapping layer strip;

(f) removing the first material and the photoresist layer;

(g) forming an oxide beside the at least one trapping layer strip and above the at least one bit line;

(h) forming at least one word line on the at least one trapping layer strip;

(i) forming a second material layer on surfaces of the at least one word line;

(j) using the second material layer as an etching mask to pattern the at least one trapping layer strip into a plurality of trapping layer block structures; and

(k) removing the second polymer.

2. (Cancelled) The method of claim 1, wherein the first material layer comprises a first polymer and the second material layer comprises a second polymer.

3. (Cancelled) The method of claim 2, wherein the trapping layer comprises in sequence, a first oxide layer, a nitride layer, and a second oxide layer, the first oxide layer, nitride layer, and second oxide layer forming an oxide-nitride-oxide (ONO) stack.

4. (Cancelled) The method of claim 3, wherein the step of patterning the trapping layer comprises patterning the oxide-nitride layer of the ONO stack only so that the first oxide layer remains substantially unpatterned.

5. (Cancelled) The method of claim 2, further comprising a step of forming a BARC layer before the photoresist layer is formed.

6. (Cancelled) The method of claim 2, wherein:
the at least one bit line comprises a plurality of bit lines;
the at least one trapping layer strip comprises a plurality of trapping layer strips; and
the at least one word line comprises a plurality of word lines.

7. (Cancelled) The method of claim 6, wherein:
the trapping layer comprises an oxide-nitride-oxide (ONO) film; and
the step of patterning the trapping layer comprises patterning the oxide-nitride layer of the ONO stack only so that the first oxide layer remains substantially unpatterned.

8. (Cancelled) A method for forming a nonvolatile memory on a semiconductor substrate, the method comprising the steps of:
(a) providing a prepared semiconductor substrate;
(b) forming a trapping layer on the semiconductor substrate;
(c) applying and patterning a photoresist over the trapping layer to form a plurality of photoresist strips;
(d) selectively implanting the semiconductor substrate to form a plurality of bit lines;

(e) forming a first material layer on surfaces of the patterned photoresist;

(f) etching back portions of the trapping layer to form a plurality of trapping layer strips;

(g) removing the first material layer and the patterned photoresist;

(h) forming an oxide over the plurality of bit lines;

(i) forming a plurality of word lines;

(j) forming a second material layer on surfaces of the word lines;

(k) etching portions of the plurality of trapping layer strips to form a plurality of trapping layer block structures; and

(l) removing the second material layer.

9. (Cancelled) The method of claim 8, wherein the first material layer comprises a first polymer and the second material layer comprises a second polymer.

10. (Cancelled) The method of Claim 9, wherein the step of forming an oxide comprises a step of growing an oxide between the trapping layer strips until a height of the oxide is about equal to a height of the trapping layer strips.

11. (Cancelled) The method of claim 9, wherein the trapping layer comprises in sequence, a first oxide layer, a nitride layer, and a second oxide layer, the first oxide layer, nitride layer, and second oxide layer forming an oxide-nitride-oxide (ONO) stack.

12. (Cancelled) The method of claim 11, wherein the second oxide layer is grown over the nitride layer, and wherein the second oxide layer consumes a portion of the nitride layer during the growth.

13. (Cancelled) The method of claim 11, wherein the etch performed in step (f) removes portions of the second oxide layer and the nitride layer only..

14. (Cancelled) The method of claim 11, wherein the etch performed in step (f) removes portions

of the second oxide layer and portions of the nitride layer, and further removes smaller portions of the first oxide layer, the portions being substantially greater than the smaller portions.

15. (Cancelled) The method of claim 9, wherein the first polymer and the second polymer are formed using a dielectric resolution enhancement coating technique.

16. (Cancelled) The method of claim 15, wherein the dielectric resolution enhancement coating technique is performed in an etcher.

17. (Cancelled) The method of claim 9, wherein the first polymer layer is used as an etch block during the etch of step (f).

18. (Cancelled) The method of claim 9, wherein the second polymer layer is used as an etch block during the etch of step (k).

19. (Cancelled) The method of claim 9, wherein the plurality of word lines are centrally disposed above corresponding members of the plurality of trapping layer block structures.

20. (Cancelled) The method of claim 9, wherein each trapping layer block structure overlaps portions of adjoining bit lines of the plurality of bit lines.

21. (Cancelled) The method of claim 9, wherein each trapping layer block structure has a greater width than a corresponding word line.

22. (Original) A nonvolatile memory on a semiconductor substrate, comprising:
(a) a prepared semiconductor substrate;
(b) a plurality of bit lines;
(c) a plurality of trapping layer block structures; and

(d) a plurality of word lines over corresponding members of the plurality of trapping layer block structures, wherein widths of the trapping layer block structures are greater than widths of the word lines.

23. (Original) The nonvolatile memory of claim 22, and further comprising at least one dielectric disposed between the plurality of word lines and trapping layer block structures.

24. (Original) The nonvolatile memory of claim 22, wherein the plurality of trapping layer block structures comprises in sequence, a first oxide layer, a nitride layer, and a second oxide layer.

25. (Original) The nonvolatile memory of claim 22, wherein the plurality of trapping layer block structures overlaps portions of adjoining members of the plurality of bit lines.